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TITLE: Cache sharing control in a multiprocessor

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INVENTOR-INFORMATION:

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US-CL-CURRENT: 711/124, 711/142 , 711/144 , 711/145

ABSTRACT:

The hybrid cache control provides a sharing (SH) flag with each line representation in each private CP cache directory in a multiprocessor (MP) to uniquely indicate for each line in the associated cache whether it is to be handled as a store-in-cache (SIC) line when its SH flag is in non-sharing state, and as a store-through (ST) cache line when its SH flag is in sharing state. At any time the hybrid cache can have some lines operating as ST lines, and other lines as SIC lines.

A newly fetched line (resulting from a cache miss) has its SH flag set to non-sharing (SIC) state in its location determined by cache replacement selection circuits, unless the SH flag for the requested line is dynamically set to sharing (ST) state and if a cross-interrogation (XI) hit in another cache is found by cross-interrogation (XI) controls, which XIs all other cache directories in the MP for every store or fetch cache miss and for every store cache hit of a ST line (having SH= 1).

A XI hit signals that a conflicting copy of the line has been found in another cache. If the conflicting cache line is changed from its corresponding MS line, the cache line is castout to MS. The sharing (SH) flag for the conflicting line is set to sharing state for a fetch miss, but the conflicting line is invalidated for a store miss.

09/17/2003, EAST Version: 1.04.0000

8 Claims, 12 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

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Brief Summary Text - BSTX (20):
If a local store miss has occurred, the **remote copy** of the conflicting line is always invalidated, because the requesting CP must store into the line after it is received by its local cache and therefore must have **exclusive control** over the line in the local cache. Therefore, the invalidation of the line in the remote cache avoids having two different versions of the same line in the MP. But only if the line was changed (CH flag is on) is the conflicting line castout to MS, and such castout occurs before the line is invalidated.

Brief Summary Text - BSTX (29):
Therefore, whenever plural CPs alternately store into a line marked as shared (SH=1) the CPs alternately take **exclusive control** over that line in MS with only one castout occurring from any cache receiving the first store request only if the CH flag is on; but with the prior EX/RO flag (which must be set to EX state while storing is being done to a line), alternate castouts to MS are required when switching control over that line from one CP cache to another CP cache. Thus, no castout ping-ponging occurs with the SH flag operation of this invention as occurs with the prior EX/RO flag operations.

Detailed Description Text - DETX (28):
FIG. 8 shows SC to CP command logic circuits for receiving a line fetch (LF) storage request on line 216 and 217 or a store through request on line 214 from FIG. 9 to provide an appropriate conflict signal command to the BCE control circuits in FIG. 10. The BCE control circuits in FIG. 10 respond by invalidating the conflicting line in its CP directory after casting out the line if it was changed. The circuits in FIG. 8 are **duplicated** in the